CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A ferroelectric or high dielectric constant capacitor electrode, comprising:

an electrode having a platinum-rhodium layer and a platinum layer on top of the platinum-rhodium layer.

2. The capacitor of claim 1, wherein the platinum-rhodium layer comprises an alloy comprising approximately 3 to approximately 40 percent rhodium.

3. The capacitor of claim 2, wherein the alloy further comprises approximately 60 to approximately 97 percent platinum.

4. The capacitor of claim 1, wherein the platinum-rhodium layer has a thickness within the range of about 100 to about 800 Angstroms.

5. The capacitor of claim 1, wherein the platinum-rhodium layer has a thickness within the range of about 150 to about 300 Angstroms.

6. The capacitor of claim 1, wherein the platinum layer has a thickness within the range of about 50 to about 300 Angstroms.

7. The capacitor of claim 1, wherein the platinum layer has a thickness within the range of about 50 to about 150 Angstroms.

8. The capacitor of claim 1, further comprising a titanium layer beneath the platinum-rhodium layer.

9. The capacitor of claim 8, wherein the titanium layer has a thickness within the range of about 60 to about 200 Angstroms.

10. The capacitor of claim 8, wherein the titanium layer has a thickness within the range of about 60 to about 100 Angstroms.

11. The capacitor of claim 8, further comprising a titanium nitride layer beneath the titanium layer.

12. The capacitor of claim 11, wherein the titanium nitride layer has a thickness within the range of about 100 to about 200 Angstroms.

13. The capacitor of claim 11, wherein the titanium nitride layer has a thickness within the range of about 100 to about 150 Angstroms.

14. A capacitor, comprising:

a lower electrode having a platinum-rhodium layer and a platinum layer on top of the platinum-rhodium layer;

an upper electrode; and

a dielectric layer of a ferroelectric or high dielectric constant dielectric material formed between said lower and upper electrodes, wherein said dielectric layer is in contact with the platinum layer of said lower electrode.

15. The capacitor of claim 14, wherein the platinum-rhodium layer comprises an alloy comprising approximately 60 to approximately 97 percent platinum.

16. The capacitor of claim 15, wherein the alloy further comprises approximately 3 to approximately 40 percent rhodium.

17. The capacitor of claim 14, wherein the platinum-rhodium layer has a thickness within the range of about 100 to about 800 Angstroms.

18. The capacitor of claim 14, wherein the platinum-rhodium layer has a thickness within the range of about 150 to about 300 Angstroms.

19. The capacitor of claim 14, wherein the platinum layer has a thickness within the range of about 50 to about 300 Angstroms.

20. The capacitor of claim 14, wherein the platinum layer has a thickness within the range of about 50 to about 150 Angstroms.

21. The capacitor of claim 14, further comprising a titanium layer beneath the platinum-rhodium layer.

22. The capacitor of claim 21, wherein the titanium layer has a thickness within the range of about 60 to about 200 Angstroms.

23. The capacitor of claim 21, wherein the titanium layer has a thickness within the range of about 60 to about 100 Angstroms.

24. The capacitor of claim 21, further comprising a titanium nitride layer beneath the titanium layer.

25. The capacitor of claim 24, wherein the titanium nitride layer has a thickness within the range of about 100 to about 200 Angstroms.

26. The capacitor of claim 24, wherein the titanium nitride layer has a thickness within the range of about 100 to about 150 Angstroms.

27. The capacitor of claim 14, wherein the upper electrode has a conductive layer.

28. The capacitor of claim 27, wherein the conductive layer is a layer of material selected from the group consisting of titanium nitride, tungsten nitride, platinum, and polysilicon.

29. The capacitor of claim 14, wherein the upper electrode has a platinum layer and a platinum-rhodium layer on top of the platinum layer.

30. The capacitor of claim 14, wherein the dielectric layer has a thickness of less than about 5000 Angstroms.

31. The capacitor of claim 14, wherein the dielectric layer has a thickness of less than about 500 Angstroms.

32. The capacitor of claim 14, wherein the dielectric material is a metallic oxide having a perovskite or ilmenite crystal structure and a dielectric constant of approximately 20 or higher.

33. The capacitor of claim 14, wherein the dielectric material is selected from the group consisting of PLZT, PST, BBT, BT, and ST.

34. The capacitor of claim 14, wherein the dielectric material is BST.

35. The capacitor of claim 14, wherein the dielectric material is PZT.

36. The capacitor of claim 14, wherein the dielectric material is SBT.

37. The capacitor of claim 14, wherein the dielectric material is tantalum pentoxide.

38. A capacitor, comprising:

a lower electrode having a titanium layer, an alloy layer on top of the titanium layer, wherein the alloy layer comprises approximately 60 to approximately 97 percent platinum and approximately 3 to approximately 40 percent rhodium, and a platinum layer on top of the alloy layer;

an upper electrode; and

a dielectric layer of a ferroelectric or high dielectric constant dielectric material formed between said lower and upper electrodes, wherein said dielectric layer is in contact with the platinum layer of said lower electrode.

39. The capacitor of claim 38, wherein the titanium layer has a thickness within the range of about 60 to about 200 Angstroms.

40. The capacitor of claim 38, wherein the titanium layer has a thickness within the range of about 60 to about 100 Angstroms.

41. The capacitor of claim 38, wherein the alloy layer has a thickness within the range of about 100 to about 800 Angstroms.

42. The capacitor of claim 38, wherein the alloy layer has a thickness within the range of about 150 to about 300 Angstroms.

43. The capacitor of claim 38, wherein the platinum layer has a thickness within the range of about 50 to about 300 Angstroms.

44. The capacitor of claim 38, wherein the platinum layer has a thickness within the range of about 50 to about 150 Angstroms.

45. The capacitor of claim 38, further comprising a titanium nitride layer beneath the titanium layer.

46. The capacitor of claim 45, wherein the titanium nitride layer has a thickness within the range of about 100 to about 200 Angstroms.

47. The capacitor of claim 45, wherein the titanium nitride layer has a thickness within the range of about 100 to about 150 Angstroms.

48. The capacitor of claim 38, wherein the upper electrode has a conductive layer.

49. The capacitor of claim 48, wherein the conductive layer is a layer of material selected from the group consisting of titanium nitride, tungsten nitride, platinum, and polysilicon.

50. The capacitor of claim 38, wherein the upper electrode has a platinum layer and a platinum-rhodium layer on top of the platinum layer.

51. The capacitor of claim 38, wherein the dielectric layer has a thickness of less than about 5000 Angstroms.

52. The capacitor of claim 38, wherein the dielectric layer has a thickness of less than about 500 Angstroms.

53. The capacitor of claim 38, wherein the dielectric material is a metallic oxide having a perovskite or ilmenite crystal structure and a dielectric constant of approximately 20 or higher.

54. The capacitor of claim 38, wherein the dielectric material is selected from the group consisting of BST, PZT, SBT, PLZT, PST, BBT, BT, ST and tantalum oxide.

55. A memory cell, comprising:

a substrate;

a transistor including a gate on said substrate and a source/drain region in said substrate disposed adjacent to said gate;

a capacitor comprising an electrode having a platinum-rhodium layer and a platinum layer on top of the platinum-rhodium layer, wherein the electrode has a lateral surface aligned with the source/drain region; and

a conductive plug providing electrical contact between the source/drain region and the lateral surface of the electrode.

56. The memory cell of claim 55, wherein the platinum-rhodium layer comprises an alloy of approximately 3 to approximately 40 percent rhodium and approximately 60 to approximately 97 percent platinum.

57. The memory cell of claim 55, wherein the platinum-rhodium layer has a thickness within the range of about 150 to about 300 Angstroms.

58. The memory cell of claim 55, wherein the platinum layer has a thickness within the range of about 50 to about 150 Angstroms.

59. The memory cell of claim 55, wherein the electrode further comprises a titanium layer beneath the platinum-rhodium layer.

60. The memory cell of claim 59, wherein the titanium layer has a thickness within the range of about 60 to about 100 Angstroms.

61. The memory cell of claim 59, wherein the electrode further comprises a titanium nitride layer beneath the titanium layer.

62. The memory cell of claim 61, wherein the titanium nitride layer has a thickness within the range of about 100 to about 150 Angstroms.

63. An integrated circuit, comprising:

an electrical circuit containing a ferroelectric or high dielectric constant capacitor, wherein the capacitor has a lower electrode having a platinum-rhodium layer and a platinum layer on top of the platinum-rhodium layer.

64. The circuit of claim 63, wherein the platinum-rhodium layer comprises an alloy of approximately 3 to approximately 40 percent rhodium and approximately 60 to approximately 97 percent platinum.

65. The circuit of claim 63, wherein the platinum-rhodium layer has a thickness within the range of about 150 to about 300 Angstroms.

66. The circuit of claim 63, wherein the platinum layer has a thickness within the range of about 50 to about 150 Angstroms.

67. The circuit of claim 63, wherein the lower electrode further comprises a titanium layer beneath the platinum-rhodium layer.

68. The circuit of claim 67, wherein the titanium layer has a thickness within the range of about 60 to about 100 Angstroms.

69. The circuit of claim 67, wherein the lower electrode further comprises a titanium nitride layer beneath the titanium layer.

70. The circuit of claim 69, wherein the titanium nitride layer has a thickness within the range of about 100 to about 150 Angstroms.

71. A computer system, comprising:

a processor; and

a memory circuit connected to the processor, the memory circuit containing at least one memory cell having a ferroelectric or high dielectric constant capacitor, wherein the capacitor has a lower electrode having a platinum-rhodium layer and a platinum layer on top of the platinum-rhodium layer.

72. A method of forming a lower electrode for a capacitor, comprising the steps of:

providing a substrate;

forming a platinum-rhodium layer on the substrate; and

forming a platinum layer on the platinum-rhodium layer.

73. The method of claim 72, wherein said platinum-rhodium layer forming step comprises chemical vapor deposition.

74. The method of claim 72, wherein said platinum-rhodium layer forming step comprises physical vapor deposition.

75. The method of claim 72, wherein said platinum-rhodium layer forming step comprises sputtering.

76. The method of claim 72, wherein said platinum-rhodium layer forming step comprises evaporation.

77. The method of claim 72, wherein said platinum-rhodium layer comprises approximately 3 to approximately 40 percent rhodium.

78. The method of claim 77, wherein said platinum-rhodium layer comprises approximately 60 to approximately 97 percent platinum.

79. The method of claim 72, wherein the platinum-rhodium layer is formed to a thickness of about 100 to about 800 Angstroms.

80. The method of claim 72, wherein the platinum-rhodium layer is formed to a thickness of about 150 to about 300 Angstroms.

81. The method of claim 72, wherein said platinum layer forming step comprises chemical vapor deposition.

82. The method of claim 72, wherein said platinum layer forming step comprises physical vapor deposition.

83. The method of claim 72, wherein said platinum layer forming step comprises sputtering.

84. The method of claim 72, wherein said platinum layer forming step comprises evaporation.

85. The method of claim 72, wherein the platinum layer is formed to a thickness of about 50 to about 300 Angstroms.

86. The method of claim 72, wherein the platinum layer is formed to a thickness of about 50 to about 150 Angstroms.

87. The method of claim 72, further comprising forming a titanium layer on the substrate prior to formation of the platinum-rhodium layer.

88. The method of claim 87, further comprising forming a titanium nitride layer on the substrate prior to formation of the titanium layer.

89. The method of claim 72, wherein said platinum-rhodium and platinum layer forming steps comprise in-situ chemical vapor deposition.

90. A method of forming a capacitor, comprising the steps of:

providing a substrate;

forming a platinum-rhodium layer on the substrate;

forming a platinum layer on the platinum-rhodium layer;

forming a dielectric layer of a ferroelectric or high dielectric constant dielectric material on the platinum layer; and

forming an upper electrode on the dielectric layer.

91. The method of claim 90, wherein said platinum-rhodium layer forming step comprises chemical vapor deposition.

92. The method of claim 90, wherein said platinum-rhodium layer comprises approximately 3 to approximately 40 percent rhodium.

93. The method of claim 92, wherein said platinum-rhodium layer comprises approximately 60 to approximately 97 percent platinum.

94. The method of claim 90, wherein the platinum-rhodium layer is formed to a thickness of about 150 to about 300 Angstroms.

95. The method of claim 90, wherein said platinum layer forming step comprises chemical vapor deposition.

96. The method of claim 90, wherein the platinum layer is formed to a thickness of about 50 to about 150 Angstroms.

97. The method of claim 90, wherein said platinum-rhodium and platinum layer forming steps comprise in-situ chemical vapor deposition.

98. The method of claim 90, further comprising forming a titanium layer on the substrate prior to formation of the platinum-rhodium layer.

99. The method of claim 98, further comprising forming a titanium nitride layer on the substrate prior to formation of the titanium layer.

100. The method of claim 90, wherein said dielectric layer forming step comprises spinning.

101. The method of claim 90, wherein said dielectric layer forming step comprises sputtering.

102. The method of claim 90, wherein said dielectric layer forming step comprises chemical vapor deposition.

103. The method of claim 90, wherein said dielectric layer forming step comprises ion beam sputtering.

104. The method of claim 90, wherein said dielectric layer forming step comprises laser beam deposition.

105. The method of claim 90, wherein said dielectric layer forming step comprises molecular beam epitaxy.

106. The method of claim 90, wherein said dielectric layer forming step comprises evaporation.

107. The method of claim 90, wherein said dielectric layer forming step comprises a sol-gel process.

108. The method of claim 90, wherein said dielectric layer is formed to a thickness of less than about 5000 Angstroms.

109. The method of claim 90, wherein said dielectric layer is formed to a thickness of less than about 500 Angstroms.

110. The method of claim 90, wherein the dielectric material is a metallic oxide having a perovskite or ilmenite crystal structure and a dielectric constant of approximately 20 or higher.

111. The method of claim 90, wherein the dielectric material is selected from the group consisting of PLZT, PST, BBT, BT, and ST.

112. The method of claim 90, wherein the dielectric material is BST.

113. The method of claim 90, wherein the dielectric material is PZT.

114. The method of claim 90, wherein the dielectric material is SBT.

115. The method of claim 90, wherein the dielectric material is tantalum pentoxide.

116. The method of claim 90, wherein said upper electrode forming step comprises forming a conductive layer on the dielectric layer.

117. The method of claim 116, wherein the conductive layer is a layer of material selected from the group consisting of titanium nitride, tungsten nitride, platinum, and polysilicon.

118. The method of claim 90, wherein said upper electrode forming step comprises forming a platinum layer on the dielectric layer and forming a platinum-rhodium layer on the platinum layer.

119. A method of forming a capacitor, comprising the steps of:

providing a substrate;

forming a first electrode on the substrate, wherein the first electrode has a titanium layer on the substrate, a platinum-rhodium layer on the titanium layer, and a platinum layer on the platinum-rhodium layer;

forming a dielectric layer of a ferroelectric or high dielectric constant dielectric material on the first electrode; and

forming a second electrode on the dielectric layer.

120. The method of claim 119, wherein said first electrode forming step further comprises forming a titanium nitride layer on the substrate prior to formation of the titanium layer.

121. The method of claim 119, wherein said second electrode forming step comprises forming a conductive layer on the dielectric layer.

122. The method of claim 119, wherein said second electrode forming step comprises forming a platinum layer on the dielectric layer and forming a platinum-rhodium layer on the platinum layer.

123. The method of claim 119, wherein said first electrode forming step comprises in-situ chemical vapor deposition.